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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,156	04/02/2001	James Broc Stirton	2000.071000	8997
23720	7590	09/23/2004	EXAMINER	
WILLIAMS, MORGAN & AMERSON, P.C. 10333 RICHMOND, SUITE 1100 HOUSTON, TX 77042				VALENTIN, JUAN D
			ART UNIT	PAPER NUMBER
			2877	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	09/824,156	Applicant(s)	STIRTON, JAMES BROCK
Examiner	Juan D Valentin II	Art Unit	2877

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 25 June 2004.
2a) This action is FINAL. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,2 and 4-37 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1,2 and 4-37 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1,2, & 4-37 rejected under 35 U.S.C. 103(a) as being unpatentable over Kleinknecht in view of Kotani (USPN '362).

Claim 1

Kleinknecht discloses in conjunction with Fig. 1, a method comprising of providing a semiconductor substrate 10 and forming a first plurality of implant regions 14 in the substrate 10. Kleinknecht discloses illuminating 18 a first plurality of implant regions 14 with a light source 26 in a scatterometry tool generating a trace profile corresponding to an implant profile of said implant regions (col. 3, lines 5-42).

Kleinknecht substantially teaches the claimed invention except that it fails to show provide a library comprised of a plurality of calculated trace profiles of implant regions having varying implant profiles. Kotani shows that it is known to provide a library comprised of a plurality of calculated trace profiles of implant regions having varying implant profiles (col. 1, lines 22-25, col. 3, line 57-col. 4, line 5 & col. 4, line 53-col. 5, line 5) for manufacturing semiconductor devices. It would have been obvious to someone of ordinary skill in the art to combine the device of Kleinknecht with the library (database) of calculated (acquired) data of

Kotani for the purposes of providing a means for managing the production of semiconductor wafers (Kotani, col. 2, lines 15-17).

In response to applicant's argument that there is no suggestion to combine the references (Remarks section, 06/25/2004, last paragraph pg. 10), the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Examiner would like to kindly point out to Applicant that motivation has been provided above with regards to the combination of Kleinknecht and Kotani and can be found in the last line of the second paragraph of the rejection to claim one above. For further clarification of the record, not only do the references pertain to the same technical field of semiconductor device manufacturing, motivation can be found within Kleinknecht (col. 4, lines 38-46), which further strengthens the motivation cited within Kotani for the combination of the two references.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning (Remarks section, 06/25/2004, first paragraph pg. 11), it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to Applicants argument that neither of the claimed references discloses the step of creating a library comprised of a plurality of calculated trace profiles of implant regions having varying implant profiles (Remarks section, 06/25/2004, first paragraph pg. 12- first paragraph pg. 14), Examiner kindly points to col. 3, line 57-col. 4, line 5 of Kotani which discloses the said limitation noted above. It is obvious to someone of ordinary skill in the art at the time of the claimed invention, that the references as disclosed by Examiner can read on the Applicants claimed limitation. Specifically starting at col. 3, line 62 where Kotani discloses “The data accumulation means 20 accumulates and stores various data which have been acquired over a long a long period of time...data accumulation means 20 also provides for reference to the accumulated data...for statistical computation using these data”. So it can be seen that Kotani uses a database i.e. library, for storing data accumulated as well as statistical computations. Going back to Kleinknecht , it can be seen that Kleinknecht discloses a plurality of calculated trace profiles of implant regions having varying implant profiles (col. 4, lines 3-19). Therefore, the combination of Kleinknecht in view of Kotani discloses Applicants claimed invention and the rejection is maintained.

Claim 2

Kleinknecht in view of Kotani discloses a method further comprising generating an additional trace profile for an additional plurality of implant regions formed in said substrate or additional substrates. The said additional plurality of implant regions having an implant profile different from said first plurality of implant regions (Kleinknecht, col. 2, line 28-col. 3, line 54). Kleinknecht in view of Kotani discloses several patterns were fabricated, and it is obvious to someone of ordinary skill in the art at the time of the claimed invention that one would want to

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obtain different implant depth profiles for different implantation depths and implant concentration levels of the several fabricated profiles in order to save considerably in man-hours needed for taking four-point sheet resistance tests (Kleinknecht, col. 2, lines 28-40 & col. 4, lines 32-46).

Claims 4-7

Kleinknecht in view of Kotani discloses a light source, a grating structure, P and N-type dopant materials, and an implant depth profile comprised of a dopant concentration level (Kleinknecht, col. 2, lines 28-40 & col. 3, lines 5-54).

Claim 8

Kleinknecht discloses in conjunction with Fig. 1, a method of measuring profiles (depth profiles) of implant regions 14 formed in a semiconductor substrate 10 comprising forming a plurality of implant regions 14 in a semiconductor substrate 10. Kleinknecht discloses illuminating 18 said plurality of implant regions and measuring light reflected off the substrate to generate a profile trace for said implant regions (col. 3, lines 5-42).

Kleinknecht substantially teaches the claimed invention except that it fails to show comparing the generated profile trace to a target profile trace and modifying based upon a deviation between the generated profile trace and the target profile trace at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates. Kotani shows that it is known to provide comparing the generated profile trace to a target profile trace and modifying based upon a deviation between the generated profile trace and the target profile trace at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (col. 1, lines 22-25, col. 3, line 57-col. 4, line 5 & col. 5,

lines 14-32) for manufacturing semiconductor devices. It would have been obvious to someone of ordinary skill in the art to combine the device of Kleinknecht with the library (database) of calculated (acquired) data of Kotani for the purposes of providing a means for managing the production of semiconductor wafers (Kotani, col. 2, lines 15-17).

In response to Applicants arguments regarding claim 8 found starting at the second paragraph of pg. 14 through the first paragraph of pg. 16 in the Remarks section dated 06/25/2004), it can be seen that Kleinknecht discloses forming a plurality of implant regions in a semiconducting substrate, illuminating and measuring light reflected off the substrate to generate a profile trace for the implant regions as shown above. Further, in combination with Kotani discloses comparing the generated profile trace to a target profile trace, and modifying, based upon a deviation between the generated profile trace and the target profile trace, at least one parameter of an ion implant process used to form implant regions on subsequently processed substrates (col. 5, lines 14-32, especially lines 14-20). It can be seen from the cited passage that Kotani discloses a data base used to store data concerning processes which have already been preformed, as well as a program for carrying out previously established process flows. To someone of ordinary skill in the art at the time of the claimed invention the cited passage provides support for feed forward process control AND also feedback process control.

Claim 9

Kleinknecht substantially teaches the claimed invention except that it fails to show provide a method comprising correlating the generated profile trace to a profile trace from a library where the profile trace from the library has an associated implant region profile. Kotani shows that it is known to provide a method comprising correlating the generated profile trace to a

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profile trace from a library where the profile trace from the library has an associated implant region profile (col. 1, lines 22-25, col. 3, line 57-col. 4, line 5 & col. 4, line 53-col. 5, line 57) for manufacturing semiconductor devices. It would have been obvious to someone of ordinary skill in the art to combine the device of Kleinknecht with the correlation (reference) of stored data from a library (database) to newly acquired data of Kotani for the purposes of providing a means for managing the production of semiconductor wafers (Kotani, col. 2, lines 15-17).

Claim 10

Kleinknecht substantially teaches the claimed invention except that it fails to show modifying based upon a deviation between the generated profile trace and a profile trace from the library, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates. Kotani shows that it is known to provide modifying based upon a deviation between the generated profile trace and a profile trace from the library, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (col. 1, lines 22-25, col. 3, line 57-col. 4, line 5 & col. 5, lines 14-32) for manufacturing semiconductor devices. It would have been obvious to someone of ordinary skill in the art to combine the device of Kleinknecht with the library (database) of calculated (acquired) data of Kotani for the purposes of providing a means for managing the production of semiconductor wafers (Kotani, col. 2, lines 15-17). It is obvious that when comparing an obtained profile trace to a previously attained profile trace, whether it's a target profile or not, both will be stored in some form of library/database in order to be used for future comparison as shown by Kotani.

Claims 11, 19, 27, & 34

Kleinknecht in view of Kotani discloses wherein measuring the reflected light comprises measuring the intensity of the reflected light (col. 3, lines 5-42).

Claims 12 & 20

Kleinknecht in view of Kotani discloses a method comprising providing a library of calculated profiles traces, each of which correspond to a unique profile of an implanted region (Kotani, col. 5, lines 14-57). It is obvious to someone of ordinary skill in the art that the process flows stored by Kotani are associated with an unique implant region profile based on a specific process flow to achieve which ever desired unique profile.

Regarding the further limitation in claim 20, it is the position of the Office that even though the reference of Kleinknecht in view of Kotani does not specifically disclose providing a library of profile traces **in a library**, it does outline the importance of storing profile characteristics in a processor (database) (col. 4, line 41-63). In light of the applicants disclosure, there is no critically distinguishing providing a **library in a library** feature in the applicants disclosure that exemplifies novelty over prior art disclosure. Therefore producing the same results as the applicant's limitation, therefore the reference of Kleinknecht in view of Kotani reads on applicants claimed limitation.

Further, claim 12 is rejected for the same reasons set forth in rejected claim 1.

Claims 13, 14, 21, 22, 28, 29, 36, & 37

Official notice taken. It is the position of the Office that it is obvious and well known to someone of ordinary skill in the art at the time of the claimed invention to anneal a semiconductor substrate during the manufacturing process, whether it be before or after an ion

implantation process. This is evident because it is well known in the art to perform optical measuring processes to inspect manufactured devices several times during the manufacturing process in order to insure successful process conditions **throughout** the **entire** process.

Claims 15, 23, & 30

Kleinknecht in view of Kotani discloses a method wherein modifying at least one parameter of an ion implant process comprises modifying at least one of an ion implant energy, an implant angle, a dopant material, and a dopant material concentration (Table 1, col. 4, Kleinknecht). It is obvious and well known to someone of ordinary skill in the art that during the fabrication process of semiconductor devices, certain process parameters such as implant angles, dopant material and dopant material concentration among others are variable in order to quickly optimize production of the semiconductor devices. Therefore, Applicant will be appreciated that the reference of Kleinknecht in view of Kotani reads on the applicants claimed limitations.

Claim 16

Kleinknecht discloses in conjunction with Fig. 1, a method of measuring profiles (depth profiles) of implant regions 14 formed in a semiconductor substrate 10 comprising forming a plurality of implant regions 14 in a semiconductor substrate 10. Kleinknecht discloses illuminating 18 said plurality of implant regions and measuring light reflected off the substrate to generate a profile trace for said implant regions (col. 3, lines 5-42).

Kleinknecht substantially teaches the claimed invention except that it fails to show provide a method comprising comparing the generated profile trace to a calculated profile trace from a library, the calculated profile trace having an associated implant region profile and modifying based upon a deviation between the generated profile trace and the calculated profile

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trace, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates. Kotani shows that it is known to provide a method comprising comparing the generated profile trace to a calculated profile trace from a library and modifying based upon a deviation between the generated profile trace and the calculated profile trace, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (col. 1, lines 22-25, col. 3, line 57-col. 4, line 5 & col. 4, line 53-col. 5, line 57) for manufacturing semiconductor devices. It would have been obvious to someone of ordinary skill in the art to combine the device of Kleinknecht with the comparison (reference) of stored data from a library (database) to newly acquired data of Kotani for the purposes of providing a means for managing the production of semiconductor wafers (Kotani, col. 2, lines 15-17). It is obvious that the stored depth profiles of Kotani are calculated prior to be stored in the database.

Further, claim 16 is rejected for the same reasons set forth in rejected independent claims 1 & 8.

Claims 17, 18, 25, & 26

Kleinknecht substantially teaches the claimed invention except that it fails to show comparing the generated profile trace to a target profile trace and modifying based upon a deviation between the generated profile trace and the target profile trace at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates. Kotani shows that it is known to provide comparing the generated profile trace to a target profile trace and modifying based upon a deviation between the generated profile trace and the target profile trace at least one parameter of an ion implantation process used to form implant regions

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on subsequently processed substrates (col. 1, lines 22-25, col. 3, line 57-col. 4, line 5 & col. 5, lines 14-32) for manufacturing semiconductor devices. It would have been obvious to someone of ordinary skill in the art to combine the device of Kleinknecht with the library (database) of calculated (acquired) data of Kotani for the purposes of providing a means for managing the production of semiconductor wafers (Kotani, col. 2, lines 15-17).

Claim 24

Kleinknecht discloses in conjunction with Fig. 1, a method of measuring profiles (depth profiles) of implant regions 14 formed in a semiconductor substrate 10 comprising forming a plurality of implant regions 14 in a semiconductor substrate 10. Kleinknecht discloses illuminating 18 said plurality of implant regions and measuring light reflected off the substrate to generate a profile trace for said implant regions (col. 3, lines 5-42).

Kleinknecht in view of Kotani discloses a method comprising providing a library of calculated profiles traces, each of which correspond to a unique profile of an implanted region (Kotani, col. 5, lines 14-57). It is obvious to someone of ordinary skill in the art that the process flows stored by Kotani are associated with an unique implant region profile based on a specific process flow to achieve which ever desired unique profile.

Kleinknecht substantially teaches the claimed invention except that it fails to show provide a method comprising comparing the generated profile trace to a calculated profile trace from said library, the calculated profile trace having an associated implant region profile and modifying based upon a deviation between the generated profile trace and the calculated profile trace, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates. Kotani shows that it is known to provide a method

comprising comparing the generated profile trace to a calculated profile trace from a library and modifying based upon a deviation between the generated profile trace and the calculated profile trace, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (col. 1, lines 22-25, col. 3, line 57-col. 4, line 5 & col. 4, line 53-col. 5, line 57) for manufacturing semiconductor devices. It would have been obvious to someone of ordinary skill in the art to combine the device of Kleinknecht with the comparison (reference) of stored data from a library (database) to newly acquired data of Kotani for the purposes of providing a means for managing the production of semiconductor wafers (Kotani, col. 2, lines 15-17). It is obvious that the stored depth profiles of Kotani are calculated prior to be stored in the database.

Further, claim 24 is rejected for the same reasons set forth in rejected independent claim 16.

Claim 31

Kleinknecht discloses in conjunction with Fig. 1, a method of measuring profiles (depth profiles) of implant regions 14 formed in a semiconductor substrate 10 comprising forming a plurality of implant regions 14 in a semiconductor substrate 10. Kleinknecht discloses illuminating 18 said plurality of implant regions and measuring light reflected off the substrate to generate a profile trace for said implant regions (col. 3, lines 5-42).

Kleinknecht substantially teaches the claimed invention except that it fails to show comparing the generated profile trace to a target profile trace and modifying based upon a deviation between the generated profile trace and the target profile trace at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates.

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Kotani shows that it is known to provide comparing the generated profile trace to a target profile trace and modifying based upon a deviation between the generated profile trace and the target profile trace at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (col. 1, lines 22-25, col. 3, line 57-col. 4, line 5 & col. 5, lines 14-32) for manufacturing semiconductor devices. It would have been obvious to someone of ordinary skill in the art to combine the device of Kleinknecht with the library (database) of calculated (acquired) data of Kotani for the purposes of providing a means for managing the production of semiconductor wafers (Kotani, col. 2, lines 15-17).

Kleinknecht in view of Kotani discloses a method wherein modifying at least one parameter of an ion implant process comprises modifying at least one of an ion implant energy, an implant angle, a dopant material, and a dopant material concentration (Table 1, col. 4, Kleinknecht). It is obvious and well known to someone of ordinary skill in the art that during the fabrication process of semiconductor devices, certain process parameters such as implant angles, dopant material and dopant material concentration among others are variable in order to quickly optimize production of the semiconductor devices. Therefore, Applicant will be appreciated that the reference of Kleinknecht in view of Kotani reads on the applicants claimed limitations.

Further, claim 31 is rejected for the same reasons set forth in rejected independent claim 8.

Claims 32 & 33

Kleinknecht substantially teaches the claimed invention except that it fails to show provide a method comprising comparing the generated profile trace to a calculated profile trace from a library, the calculated profile trace having an associated implant region profile and

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modifying based upon a deviation between the generated profile trace and the calculated profile trace, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates. Kotani shows that it is known to provide a method comprising comparing the generated profile trace to a calculated profile trace from a library and modifying based upon a deviation between the generated profile trace and the calculated profile trace, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (col. 1, lines 22-25, col. 3, line 57-col. 4, line 5 & col. 4, line 53-col. 5, line 57) for manufacturing semiconductor devices. It would have been obvious to someone of ordinary skill in the art to combine the device of Kleinknecht with the comparison (reference) of stored data from a library (database) to newly acquired data of Kotani for the purposes of providing a means for managing the production of semiconductor wafers (Kotani, col. 2, lines 15-17). It is obvious that the stored depth profiles of Kotani are calculated prior to be stored in the database.

Claim 35

Kleinknecht in view of Kotani further discloses a method comprising providing a library of historical profile traces, each of which correspond to a unique profile of an implanted region (Kleinknecht, col. 5, lines 14-57). It is the position of the Office that adding the further limitation of **historical** profile traces does not add patentable weight, therefore, the reference of Kleinknecht in view of Kotani reads on the claimed limitations.

Response to Arguments

2. Applicant's arguments filed 06/25/2004 have been fully considered but they are not persuasive. Examiner has addressed the issues raised by Applicant with regards to claims 1-37 above.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan D Valentin II whose telephone number is (571) 272-2433. The examiner can normally be reached on Mon.-Fri..

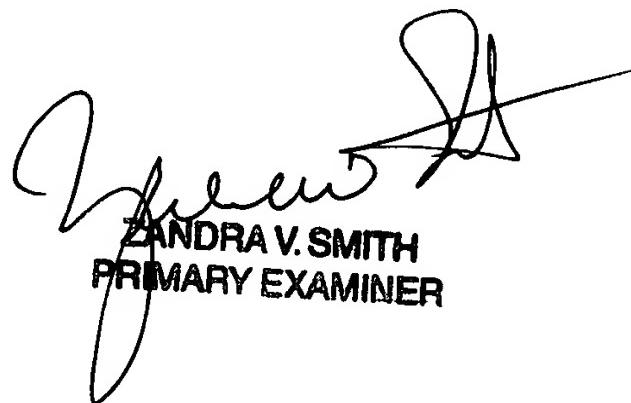
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory J Toatley, Jr. can be reached on (571) 272-2800 ext. 77. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Juan D Valentin II
Examiner 2877
JDV
September 9, 2004



SANDRA V. SMITH
PRIMARY EXAMINER